# RESEARCH

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# Performance and harmonic detection algorithm of phase locked Loop for parallel APF

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## Abstract

As the boost of power electronics technology, the harmonic problem in the power system is becoming increasingly prominent. Fourier decomposition is performed on the load current in the power system, and components with a frequency that is an integer multiple of the fundamental wave are referred to as harmonic components. Harmonic control is essential to establish a safe and reliable power grid environment and provide high-quality and clean electricity to power users. The study focused on parallel active power filters, proposed a specific harmonic detection method on the grounds of synchronous harmonic rotating coordinate system, and developed a phase-locked loop design on the grounds of order generalized integrator. Meanwhile, a compensation current control method on the grounds of space vector pulse width modulation was introduced. The results showed that in the full compensation simulation experiment, the compensated A-phase grid side current waveform was significantly improved and presented a sinusoidal shape. After 0.05 s, the actual output compensation current closely followed the command current. Meanwhile, after compensation, the total harmonic distortion rate decreased from 26.58 to 3.06%. In specific harmonic compensation simulation experiments, when the sum of 5th, 7th, and 11th harmonic components was used as the command current for compensation, the distortion of the current waveform was improved after the load undergoes a sudden change. After compensation, the 5th, 7th, and 11th harmonic content significantly decreased, and the total harmonic distortion rate decreased to 4.08%. This indicated that the proposed phase-locked loop design and harmonic detection method for active power filters had high stability and effectiveness. The study's primary contribution is to enhance the utilization efficiency of DC voltage and improve the dynamic response ability of current. Additionally, it offers a new method for reducing the impact of harmonics on the power grid and improving power quality. It provided an effective method reference for technological progress in related fields such as power electronics and control engineering.

**Keywords** Parallel APF, Phase locked loop, Harmonic detection, Synchronous harmonic rotating coordinate system, Second-order generalized integrator



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## Introduction

As the boost of industrial technology, the large-scale utilization of new power electronic equipment has brought harmonic pollution and power quality problems to the power grid (PG) (Hoevenaars et al. 2020). Various high-power rectifiers, inverters, frequency converters, and other power electronic equipment are commonly used in industrial production. However, the increasing use of various nonlinear loads on the user side, such as frequency converters and arc furnaces, generates a large number of harmonic component (HC) during operation. Therefore, it is necessary to adopt effective methods for harmonic control. At present, harmonic control mainly adopts two methods: active and passive (Gali et al. 2021). The proactive governance strategy aims to eliminate the harmonics generated by the harmonic source itself, control the power factor to 1, and is suitable for the main harmonic source in the PG, such as power electronic devices. Although this method could decrease the generation of harmonics, it cannot be completely eliminated. Passive governance is achieved by installing compensation devices near the harmonic source to compensate for harmonics in the system and prevent harmonic currents from flowing into the PG. This method is currently the main harmonic control method, but there are still some defects and limitations [3-4]. To address such issues, a parallel active power filter (APF) was introduced, which detects the HC in the load side current and injects compensation current into the PG for filtering out the HCs in the current and compensate for reactive power (RP). Meanwhile, corresponding phase-locked loops (PLL), specific harmonic detection methods, and compensation current control methods were studied and designed. The parallel APF structure connects the APF to the PG in parallel through reactors. It detects HCs in the load side current and injects compensation current into the PG to filter out the HCs in the current and compensate for reactive power. This structure is suitable for environments with inductive harmonic sources. Additionally, reactive power compensation and imbalance suppression functions can be implemented as necessary using flexible compensation methods. The contribution of the research lies in the introduction of a PLL structure on the grounds of second-order generalized integrators. The traditional synchronous rotating frame phase locked loop (SRF-PLL) solves the problem of large frequency fluctuations in the output, which helps to ensure the accuracy of the output phase. Meanwhile, a specific harmonic current detection (HCD) method on the grounds of synchronous harmonic rotation coordinate system (SHRCS) has been introduced, which helps to achieve the separation and detection of multiple harmonics. The research content includes four parts. The first part provides an overview of APF, PLL, and harmonic detection methods. The second part introduces the performance of PLL and harmonic detection algorithm for parallel APF. The first section introduces a specific HCD method on the grounds of SHRCS, and the second section introduces SRF-PLL design. The third section introduces the compensation current control method on the grounds of space vector pulse width modulation (SVPWM). The third part conducts simulation experiments to verify the proposed method in the research. The fourth part summarizes the results and proposes future prospects.

HCD is a crucial step in the operation of APF, and its detection accuracy directly affects the compensation performance of APF. Pan G and other scholars proposed a system level harmonic suppression method that does not require phase synchronization to address the issue of multi bus phase synchronization in existing system level harmonic

reduction methods. The results indicate that this method can achieve good harmonic compensation performance and ensure that the distortion rate of multi bus harmonic voltage in the PG meets the standard (Pan et al. 2021). Li Z et al. proposed an interesting view correction method to address the relationship between detection accuracy and effectiveness of single-phase parallel APF HCD. The results show that improving detection accuracy can enhance the effectiveness of detection when the load current undergoes periodic changes, while the opposite is true when the load current undergoes non periodic changes (Li et al. 2022). Researchers such as El Rahman A found that traditional ip iq harmonic detection methods have slow response and low accuracy. Therefore, they proposed a harmonic detection method on the grounds of the double second-order sliding window discrete Fourier transform. This method combines SOGI-PLL and half cycle sliding window iteration, reducing computational complexity and improving detection accuracy. The outcomes showcase that the method possesses a fast response speed and high detection accuracy, which verifies its effectiveness (El-Rahman et al. 2020). Researchers such as Prabakaran S proposed an adaptive HCD method on the grounds of neural networks to address the issue of improving the detection performance of APFs. This method utilized adaptive noise cancellation technology to separate harmonic currents from the load current. The results show that this method can still maintain highprecision HCD performance under sudden load changes (Prabakaran et al. 2020). To solve the problem of poor HCD performance, scholars such as Qiankun LI proposed an active filter method on the grounds of fixed step minimum mean square algorithm and embedded low pass filter (LPF). It used the sparrow search algorithm to improve the filtering parameters and verifies its applicability under different load values. The Matlab simulation results showcase that the SSA algorithm can decrease the current THD to below 5% (Qiankun and Yili 2022).

At present, SOGI method and synchronous rotating coordinate system (SRCS) transformation method are widely used in harmonic and vibration problems of power systems. To solve the DC offset problem in digital implementation of parallel SOGIs, scholars such as Zheng H proposed an improved pulse invariance method to discretize SOGIs. Meanwhile, LPFs were introduced to eliminate the DC offset of discrete SOGI. The results showed that the method exhibits zero AC error and good dynamic characteristics (Zheng et al. 2022). Guo M et al. proposed two frequency feeding methods independent of PLL to meet the demand of SOGI for grid voltage and frequency information in single-phase systems. Type A used cascaded recursive discrete Fourier transform and inverse recursive discrete Fourier transform for normalization, while type B used SOGI output for normalization. The results showed that both methods perform better than traditional PLL methods under transient and steady-state grid voltage disturbances (Guo et al. 2021). Cui P and other researchers discovered the synchronization and multi frequency harmonic vibration problems of maglev control torque gyroscopes in high-performance satellite platforms, and therefore proposed a control algorithm on the grounds of multi SRCS transformation. This algorithm utilized displacement sensors with orthogonal characteristics to output signals and simultaneously suppress vibrations in both directions through a controller. The results showed that this method can achieve high-precision and fast response harmonic vibration suppression (Cui et al. 2021). Song Z et al. proposed a harmonic current suppression method on the grounds of synchronous rotation coordinate transformation and adaptive filtering algorithm to address the issues of air gap magnetic field distortion and inverter nonlinearity in high-speed and precision applications of permanent magnet synchronous motors. The outcomes demonstrated the correctness and effectiveness (Song et al. 2021).

Amin et al. proposed a single-phase grounding fault location algorithm for distribution networks based on the differential equation method for measuring the fundamental frequency. The algorithm used the alternating transient program Draw to simulate the network model. The results showed that the method reduced the impact of HCs on fault location (Amin et al. 2023). To address the issue of potential distortion of fault signals due to distributed generators, Yuan J utilized a single-phase grounding fault feeder detection method for distribution networks that is based on correlation analysis and harmonic energy. The effectiveness of this method was confirmed through simulation results and actual data testing (Yuan et al. 2022). To mitigate the negative impact of electrical equipment failures, transformer overheating, and other issues on power quality, Mishra et al. utilized common coupling points to feed compensation currents into threephase (TP) systems. This improved the balance and sinusoidal grid currents, resulting in reduced harmonic distortion (Mishra et al. 2022).

According to research by numerous scholars, significant progress has been made in algorithms such as predictive control and artificial neural network control for the performance of PLL and harmonic detection methods. However, due to their complexity, these algorithms are still relatively uncommon in practical applications. Currently, an important research direction is the composite control method that combines two control methods simultaneously, utilizing the strengths of both methods to improve the shortcomings of one method. The research employs a HCD algorithm based on instantaneous reactive power theory to detect and separate various HCs. An analysis was conducted on the influence of parameters such as DC side capacitance, DC side voltage, and connecting inductance on the compensation effect. The main circuit parameter design and selection were completed. The research's primary contribution is to enhance the efficiency of DC voltage utilization and improve the current's dynamic response capability. Additionally, it offers a new method for reducing the impact of harmonics on the PG and improving power quality.

In summary, numerous researchers conducted extensive research on HCD in APF and have achieved certain results. On this basis, this study introduced a multi SRCS transformation HCD method and proposes a PLL design method on the grounds of SOGI. This is for reducing the impact of harmonics on the PG and further improve the stability and reliability of the power system.

## Harmonic detection and PLL design for parallel APF

This study first presents a specific HCD method on the grounds of the theory of instantaneous RP, using a synchronous harmonic rotating coordinate system. Subsequently, to provide accurate phase information to the transformation matrix, the SOGI-PLL method is introduced in the study. Finally, the SVPWM method is proposed to achieve APF control, and a harmonic detection method on the grounds of DC side voltage control is proposed.

#### Harmonic detection algorithm on the grounds of instantaneous RP theory

According to the working principle of APF, accurately obtaining the instruction current is a necessary condition for achieving harmonic compensation. Due to the characteristics of harmonic distribution, higher requirements are placed on the speed and dynamic performance of harmonic detection methods. In response to this issue, the instantaneous RP theory is introduced and corresponding harmonic detection methods are proposed. It assumes that the voltage values of each phase in a TP circuit are  $e_a$ ,  $e_b$ , and  $e_c$ , and the instantaneous values of current are  $i_a$ ,  $i_b$ , and  $i_c$ , respectively. After coordinate transformation, it is converted into instantaneous values of voltage and current vectors in the  $\alpha$ - $\beta$  coordinate system. On the grounds of the theory of instantaneous RP, two detection methods, p-q method and  $i_p$ - $i_q$  method, are proposed, both of which belong to the fundamental wave extraction algorithm. The core of this algorithm is for extracting the fundamental component from the signal to be detected, and obtain the harmonic command signal by subtracting the fundamental component from the original signal. But its disadvantage is that detecting harmonic currents as a whole cannot achieve the separation of specific sub harmonics [17-18]. As an active device, APF has limited bandwidth and insufficient compensation ability for high-order harmonics. According to the analysis of harmonic characteristics, the harmonics in the power system are mainly concentrated at 6 K±1 order, and the harmonic content is inversely proportional to the quantity of harmonics. The higher the quantity of harmonics, the smaller the content, and the lower the harm to the PG. Therefore, for high-order harmonics, they can be filtered out through passive devices or not compensated. For low order harmonics with high content and high harm, compensation can be achieved through parallel APF. When the capacity of the compensation device is limited, if all HCs are used as command currents, it may lead to inaccurate limiting compensation of the compensation current. In actual distribution networks, the harmonic composition and amplitude values of each harmonic are variable, so selective compensation is more flexible than full compensation (Mahmoudi et al. 2021). In response to the above characteristics, an improved SHRCS detection method on the grounds of the ip-iq method is proposed to achieve the detection of specified harmonics. The coordinate transformation for synchronous rotation expresses the mathematical relationship between electromagnetic quantities, such as voltage, current, and magnetic flux, and mechanical quantities, such as torque and speed, in a synchronous motor. This transformation is essential for conducting dynamic analyses of synchronous motors and power systems. The mathematical model commonly used for synchronous motors in power systems comprises two parts: the circuit equation of synchronous motors and the rotor motion equation. The principle of SHRCS detection method is showcased in Fig. 1.

In Fig. 1,  $U_{abc}$  represents the grid voltage, which is detected by PLL to obtain realtime phase information of the grid.  $i_{La}$ ,  $i_{Lb}$  and  $i_{Lc}$  represent the load current, which is transformed into a stationary vector by a specified multiple of the fundamental angular frequency. Using a LPF to filter out higher-order harmonics, the DC component of the specified harmonic is obtained. Then, the specified harmonic command current is obtained by inverse transformation, achieving the separation of the specified harmonic. Among them,  $C_{\alpha\beta-pqn}$  represents the transformation matrix, and  $C_{pqn-\alpha\beta}$  represents the inverse transformation matrix (Mohamad et al. 2023). It assumes that the TP current is symmetrical, and the representation of the load current is shown in Eq. (1).



Fig. 1 Schematic diagram of the SHRCS detection method

$$\begin{cases}
i_{La} = \sum_{n=1}^{\infty} \sqrt{2} I_n \sin(n\omega t + \varphi_n) \\
i_{Lb} = \sum_{n=1}^{\infty} \sqrt{2} I_n \sin(n(\omega t - 120^\circ) + \varphi_n) \\
i_{Lc} = \sum_{n=1}^{\infty} \sqrt{2} I_n \sin(n(\omega t + 120^\circ) + \varphi_n)
\end{cases}$$
(1)

In Eq. (1),  $\omega t$  represents angular velocity and  $\varphi$  represents phase angle. n represents the number of harmonics. When n = 3k + 1, the order of the TP harmonics A, B, and C lags in sequence, that is, positive sequence harmonics. When n = 3k - 1, the TP harmonic sequence leads in sequence, that is, the negative sequence harmonic. When n = 3k, the TP harmonics have the same phase, which is called zero sequence harmonics. Through a LPF, the DC component can be gotten, which is represented as Eq. (2).

$$\begin{bmatrix} i^*_{pn} \\ i^*_{qn} \end{bmatrix} = \sqrt{3} \begin{bmatrix} \pm I_n \cos \varphi_n \\ -I_n \sin \varphi_n \end{bmatrix}$$
(2)

 $i_{pn}^*$ ,  $i_{qn}^*$  represents the DC component after LPF. After inverse coordinate transformation, the specified HC can be obtained, and its calculation is shown in  $\int i_{pkn} = \sqrt{2}L_r \sin(\pm n\omega t \pm \omega_r)$ 

$$\operatorname{Eq. (3).} \begin{cases}
 I_{ahn} = \sqrt{2}I_n \sin(\pm n\omega t + \varphi_n) \\
 i_{bhn} = \sqrt{2}I_n \sin(\pm n\omega t + \varphi_n \mp 120^\circ) \\
 i_{chn} = \sqrt{2}I_n \sin(\pm n\omega t + \varphi_n \pm 120^\circ)
 (3)$$

This method can achieve the separation of specified harmonics. If multiple harmonics need to be compensated, a multi harmonic detection structure can be constructed, as shown in Fig. 2. In Fig. 2, the yellow triangle represents the fundamental phase, and sin cos represents the reference phase.  $C_{abc-pqn}$  represents the transformation matrix, and  $C_{abc-pq7}^{-1}$  represents the inverse transformation matrix.  $K_n$  represents the damping coefficient.  $i_h$  is the final command current. After extracting the fundamental phase from the PLL, a specified harmonic reference phase is obtained to participate in coordinate operation. LPF and inverse coordinate transformation are used to achieve separation detection of multiple harmonics. This method allows for the combination of a certain harmonic current or several harmonic currents as needed to ultimately obtain the instruction current. At the same time, it can accurately limit the amplitude control of each harmonic, allowing for more flexible use of the APF's capacity.



Fig. 2 HCD structure of the multi-synchronous rotation coordinate system

### PLL design on the grounds of SOGI

To achieve accurate HCD and compensation, it is essential for getting accurate frequency and phase information of the grid voltage. Therefore, a PLL link is needed to provide accurate phase information to the transformation matrix. The TP PLL structure can be regarded as a phase negative feedback system. The system mainly contains three parts: a phase detector, a loop filter, and a voltage controlled oscillator (Achlerkar and Panigrahi 2021). The phase detector is responsible for comparing the phase of the input voltage with the output phase signal, and generating a phase error signal. The loop filter will filter out the high-frequency interference in the phase error signal, while the voltage controlled oscillator will gradually approximate the phase of the output signal to the phase of the input voltage. When the output phase error signal of the phase detector is zero, it indicates that the PLL has successfully locked the phase, and the output signal is the phase signal of the input voltage. In practical applications, the voltage of the PG will exhibit imbalance due to voltage fluctuations, which will have an impact on the output results of the PLL. Under ideal conditions, the voltage balance of the TP PG is achieved by performing the Park Clark transformation on the voltage in the TP coordinate system, as shown in Eq. (4).

$$\begin{cases} \begin{bmatrix} e_{\alpha} \\ e_{\beta} \end{bmatrix} = C_{32} \begin{bmatrix} e_{a} \\ e_{b} \\ e_{c} \end{bmatrix} = e_{0} \begin{bmatrix} \cos \omega t \\ \sin \omega t \end{bmatrix} \\ \begin{bmatrix} e_{d} \\ e_{q} \end{bmatrix} = C_{park} \begin{bmatrix} e_{\alpha} \\ e_{\beta} \end{bmatrix} = e_{0} \begin{bmatrix} \cos(\omega t - \theta) \\ \sin(\omega t - \theta) \end{bmatrix}$$
(4)

In Eq. (4),  $e_a$ ,  $e_b$ , and  $e_c$  represent TP unbalanced voltage.  $e_\alpha$ ,  $e_\beta$  represents  $\alpha$ - $\beta$  Voltage in the coordinate system. When the d-axis coincides with the voltage vector (VV), there are  $\omega t = \theta$ ,  $e_d = e_0$ ,  $e_q = e_0$ . By adjusting  $e_q$  to 0 through a PI regulator, the accurate phase of the grid voltage can be obtained. The coordinate transformation stage can be regarded as a PLL phase detector module, which outputs the  $e_q$  signal. The voltage controlled oscillator is implemented by an integral stage, which outputs the phase signal

and serves as the feedback signal of the phase detector to form a closed-loop. The PI regulator acts as a loop filter stage. Based on the above analysis, it can be concluded that accurate calculation of voltage phase can be achieved under the premise of voltage balance in TP PGs. However, in practical applications, voltage imbalances in the PG can affect the output results of the PLL due to voltage fluctuations. The study focuses on TP three wire systems, and the representation of TP unbalanced voltage is shown in Eq. (5).

$$\begin{bmatrix} e_{a} \\ e_{b} \\ e_{c} \end{bmatrix} = e_{0}^{+} \begin{bmatrix} \cos(\omega t + \varphi_{0}) \\ \cos(\omega t + \varphi_{0} - 120^{\circ}) \\ \cos(\omega t + \varphi_{0} + 120^{\circ}) \end{bmatrix} + e_{0}^{-} \begin{bmatrix} \cos(-\omega t + \varphi_{1}) \\ \cos(-\omega t + \varphi_{1} - 120^{\circ}) \\ \cos(-\omega t + \varphi_{1} + 120^{\circ}) \end{bmatrix}$$
(5)

In Eq. (5),  $e_0^+$  and  $e_0^-$  represent the amplitude of the positive and negative (PAN) sequence components, and  $\varphi_0$  and  $\varphi_1$  represent the initial phase angle of the PAN sequence components. It then performs Clark and Park transformations on the PAN sequence components, where the Clark transformation is shown in Eq. (6).

$$\begin{bmatrix} e_{\alpha} \\ e_{\beta} \end{bmatrix} = C_{abc-\alpha\beta} \begin{bmatrix} e_{a} \\ e_{b} \\ e_{c} \end{bmatrix} = e_{0}^{+} \begin{bmatrix} \cos(\omega t + \varphi_{0}) \\ \sin(\omega t + \varphi_{0}) \end{bmatrix} + e_{0}^{-} \begin{bmatrix} \cos(-\omega t + \varphi_{1}) \\ \sin(-\omega t + \varphi_{1}) \end{bmatrix}$$
(6)

The Park transformation is shown in Eq. (7).

-

$$\begin{bmatrix} e_d \\ e_q \end{bmatrix} = C_{park} \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = e_0^+ \begin{bmatrix} \cos(\omega t + \varphi_0 - \theta) \\ \sin(\omega t + \varphi_0 - \theta) \end{bmatrix} + e_0^- \begin{bmatrix} \cos(-\omega t + \varphi_1 - \theta) \\ \sin(-\omega t + \varphi_1 - \theta) \end{bmatrix}$$
(7)

In Eq. (7),  $\theta$  represents the phase angle of the positive sequence component output by the PLL, which is calculated as shown in Eq. (8).

$$\theta \approx \omega t + \varphi_0 \tag{8}$$

This study substituted Eq. (8) into Eq. (7) to obtain Eq. (9).

$$\begin{bmatrix} e_d \\ e_q \end{bmatrix} = e_0^+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} + e_0^- \begin{bmatrix} \cos(-2\omega t + \varphi_1 - \varphi_0) \\ \sin(-2\omega t + \varphi_1 - \varphi_0) \end{bmatrix}$$
(9)

In Eq. (9),  $e_d$  and  $e_q$  respectively represent the voltage components of the d and q axes. When the TP is unbalanced, because of the presence of the fundamental negative sequence component, an error signal of doubling the fundamental frequency will be generated. In addition, when there are harmonics and DC bias in the grid voltage, it can also cause voltage fluctuations, thereby affecting the detection accuracy of the PLL (Wellendorf et al. 2023). A PLL design method on the grounds of second order generalized integrator (SOGI) is studied to address this issue. The second-order generalized integrator is a high-precision frequency locking technique used in power electronic control systems. It can track and phase shift specific frequency AC components, and can be used to achieve PAN sequence separation and filtering of voltage signals. Additionally, the second-order generalized integrator can generate a 90° phase shift of the PG voltage signal and has unique filtering characteristics that filter out the second HC in the d and q axes, achieving accurate phase locking. Additionally, it can detect specific

harmonics by adjusting the input frequency. The relevant structure of SOGI is showcased in Fig. 3.

In Fig. 3, K represents the damping coefficient, which contains two output signals with a difference of  $\pi/2$ , indicating an orthogonal signal. The transfer function of the two output signals is shown in Eq. (10).

$$\begin{cases} D(s) = \frac{K\omega_0 s}{s^2 + K\omega_0 s + \omega_0^2} \\ Q(s) = \frac{K\omega_0^2}{s^2 + K\omega_0 s + \omega_0^2} \end{cases}$$
(10)

In Eq. (10), s represents the complex frequency. D(s) represents amplitude frequency, Q(s) represents phase frequency. The study sets  $s = j\omega$  and calculates the amplitude frequency characteristics of the transfer function as shown in Eq. (11).

$$\begin{cases} |D(j\omega)| = \frac{K\omega_0\omega}{\sqrt{(\omega^2 - \omega_0^2) + (K\omega\omega_0)^2}} \\ \angle D(j\omega) = \angle \arctan(\frac{\omega^2 - \omega_0^2}{K\omega\omega_0}) \end{cases}$$
(11)

The calculation of phase frequency characteristics is shown in Eq. (12).

$$\begin{cases} |Q(j\omega)| = \frac{\omega}{\omega_0} |Q(j\omega)| \\ \angle Q(j\omega) = \angle Q(j\omega) - \frac{\pi}{2} \end{cases}$$
(12)

In Eq. (12), when  $\omega = \omega_0$ , there is  $|D(j\omega)| = |Q(j\omega)| = 1$ , which indicates that the output amplitude remains unchanged. The operating frequency of SOGI is set to second harmonic, specifically designed to filter out second harmonic interference caused by the fundamental negative sequence component. The structure of SOGI-PLL is showcased in Fig. 4. In Fig. 4, the operating frequency of SOGI is the second harmonic, which can filter out the second harmonic interference caused by the fundamental negative sequence component. Interference caused by the fundamental negative sequence component. Interference occurs on the d and q axes after coordinate transformation when there are harmonics in the voltage of the PG. This problem can be effectively



Fig. 3 A schematic view of the SOGI



Fig. 4 PLL structure on the grounds of SOGI

solved by adjusting the operating frequency of SOGI, achieving tracking and filtering of each frequency.

### Control algorithm on the grounds of SVPWM

In a parallel APF, the harmonic detection stage outputs a compensation current command signal, and the control circuit generates a PWM signal on the grounds of this command signal to control the opening and closing of the switching device. Due to the use of a voltage type PWM inverter as the main circuit of the parallel APF in the study, the control method of the APF is equivalent to the control method of the PWM inverter (Brosch et al. 2022). In response to this issue, this study introduces SVPWM, a novel modulation method used to control the working state of switching devices on the grounds of the output space voltage or current vector of the inverter. The output voltage of the parallel APF is represented by Eq. (13).

$$\begin{cases} U_{a0} = \left[S_a - \frac{1}{3}(S_a + S_b + S_c)\right] U_{dc} \\ U_{b0} = \left[S_b - \frac{1}{3}(S_a + S_b + S_c)\right] U_{dc} \\ U_{c0} = \left[S_c - \frac{1}{3}(S_a + S_b + S_c)\right] U_{dc} \end{cases}$$
(13)

In Eq. (13), S represents the switch and  $U_{dc}$  represents the DC side voltage.  $U_{a0}$ ,  $U_{b0}$  and  $U_{c0}$  respectively represent the output voltage components in the coordinate system. The six switching tubes in a parallel APF have eight different combinations of switch states, which correspond to the vector of the AC side voltage. The vector  $U_k$  is used to represent the different switch combination states, where the modes of  $U_0(000)$  and  $U_7(111)$  are zero, known as the zero vector. The distribution of each spatial vector on the complex plane is shown in Fig. 5. In Fig. 5, in terms of the principle of vector synthesis, the reference VV of any sector on the complex plane can be synthesized using the two non-zero vectors and zero vectors of its sector.

In real-time control, the reference VV U\* is first projected onto the  $\alpha$ - $\beta$  coordinate system, and the positional relationship between UA and UB in different sectors is further analyzed. The study introduced variables A, B, and C. When  $U_{\beta} > 0$ , the study set A=1, otherwise A=0. When  $U_{\beta} < \sqrt{3}U_{\alpha}$ , this study sets B=1, otherwise B=0. When  $U_{\beta} < -\sqrt{3}U_{\alpha}$ , this study sets C=1, otherwise C=0. The definition of N value is shown in Eq. (14).

$$N = A + 2B + 4C \tag{14}$$



Fig. 5 Plot of the spatial vector distribution in the complex plane

 Table 1
 The N values correspond to the sector codes

N	1	2	3	4	5	6	
Section	II	VI	I	IV		V	

It establishes a correspondence between N value and sector number, as shown in Table 1. By calculation, the N value of region I is 3, region II is 1, region III is 5, region IV is 4, region V is 6, and region VI is 2.

It then calculates the action time of the spatial VV. Taking the VV U\* in the first sector as an example, according to the volt second balance, Eq. (15) can be obtained.

$$|\mathbf{U}^*| = \frac{T_1}{T} |U_1| + \frac{T_2}{T} |U_2|$$
(15)

In Eq. (14), T represents the switching period of PWM, and  $T_1$  and  $T_2$  respectively represent the duration of the VVs  $U_1$  and  $U_2$  in the first sector within one switching period. The angle between the VV U<sup>\*</sup> and  $U_1$  is denoted as  $\delta$ , and Eq. (16) can be obtained.

$$\frac{T_1 \cdot |U_1|}{T \cdot \sin(\pi/3 - \delta)} = \frac{T_2 \cdot |U_2|}{T \cdot \sin(\delta)} = \frac{|U^*|}{\sin 2\pi/3}$$
(16)

This study substitutes into Eq. (15) to obtain Eq. (17).

$$\begin{cases} T_1 = \sqrt{3}T\sin(\pi/3 - \delta)\frac{|\mathbf{U}^*|}{\mathbf{U}_{dc}} \\ T_2 = \sqrt{3}T\sin\delta\frac{|\mathbf{U}^*|}{\mathbf{U}_{dc}} \end{cases}$$
(17)

This study projects U\* onto the  $\alpha$ - $\beta$  coordinate system to obtain Eq. (18).



Fig. 6 Harmonic detection method on the grounds of DC side voltage control

Table 2 Simulation pa	arameters of the system
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Module	Parameter		
Inductance of rectified bridge	1 mH		
Three-phase grid voltage	Phase voltage 220 V, Frequency 50 Hz		
The APF AC-side inductance	3 mH		
DC side voltage	700 V		
DC side capacitance	1500 μF		
Resistance to perceptual load	30 Ω1mH		
Simulation step size	1*10 <sup>-5</sup> s		

$$\begin{cases} T_1 = \frac{T}{2U_{dc}} (3U_\alpha - \sqrt{3}U_\beta) \\ T_2 = \sqrt{3} \frac{TU_\beta}{U_{dc}} \end{cases}$$

$$\tag{18}$$

To ensure good compensation current following performance of the system, it is necessary for controlling the DC side voltage of the inverter within an appropriate range to avoid overcompensation or under compensation problems caused by significant voltage fluctuations. This study mainly adopts closed-loop control method, which utilizes the structure of the main circuit itself for appropriate control to achieve stable DC side voltage. Presently, the PI control method is extensively utilized in the control of DC side voltage. It mainly compares the DC side voltage value  $U_{dc}$  with the set target value  $U_{dc}^*$ and calculates the deviation value, and then inputs this difference into the PI regulator. The adjusted current  $\Delta i_p$  is used as the input signal for the d-axis, while the input signal for the q-axis is fixed at 0. The calculated signal is added to the instruction current through inverse coordinate transformation. Through this method, during the energy exchange between the AC and DC sides, the DC capacitor voltage can be maintained in a stable state. The harmonic detection method on the grounds of DC side voltage control is showcased in Fig. 6.

## Performance analysis of PLL and harmonic detection algorithm for parallel APF

This study first analyzes the output frequency and phase waveform of SOGI-PLL, and verifies its stationarity. Then, by analyzing the detection results of each harmonic current, the effectiveness of the specific HCD method on the grounds of the SHRCS is verified. Finally, a comparative simulation experiment is conducted between full compensation and specific harmonic compensation.

#### Performance of PLL and analysis of harmonic detection algorithms

Aiming at evaluating the effectiveness of the proposed APF HCD method, PLL design, and current tracking control algorithm, a simulation model is constructed using Matlab/Simulink to verify the proposed method. The simulated power system's main circuit comprises a TP programmable voltage module and a load module. The load module is a TP uncontrolled rectifier bridge with a resistive-inductive load. To simulate load imbalance, a single-phase load is added. An inductor is connected in series on the AC side of the load for filtering. The active filtering module comprises two parts: the main circuit module and the pulse logic control module. The main circuit module is connected to the PG in parallel through inductors, and the circuit breaker controls the duration of the grid connection. The control module comprises modules for harmonic detection, compensation current tracking control, and DC side voltage control. Two methods are used for harmonic detection: the ip-iq method and specific harmonic detection. The ip-iq method uses PLL technology to isolate the influence of abnormal variables on the detection, resulting in relatively high detection accuracy. The detection of subharmonics is primarily determined by the cutoff frequency of the LPF. A lower cutoff frequency provides better filtering but also introduces significant delay. Therefore, a compromise must be made when selecting the cutoff frequency. The simulation parameters are showcased in Table 2. The parameters in Table 2 are calculated based on the main circuit parameters. The DC side voltage magnitude determines the output capability of the compensation circuit. A higher voltage results in a greater rate of change of the compensation current, which strengthens the tracking ability of the instruction circuit and improves the compensation effect. However, as the voltage level increases, so does the loss, capacitance volume, and voltage resistance requirements for switching devices. This increase in cost is not conducive to system design. Therefore, it is necessary to select a reasonable value for the DC side voltage. The stability of the DC side voltage can significantly impact system performance. To ensure optimal compensation current, it is necessary to avoid significant fluctuations in the DC side voltage, which are related to the capacitance value. If the capacitance value is too small, the voltage of the DC side bus will fluctuate excessively during load changes. A capacitance value that is too large can decrease the dynamic performance of the system and increase costs. When selecting a capacitance value, it is important to consider the impact of voltage fluctuation, tracking performance, and cost simultaneously. Connecting inductors play a crucial role in storing energy and filtering current during operation. This reduces the content of switching ripple current in the compensation current while bearing a certain fundamental voltage. The larger the inductance value, the better the filtering effect on ripple current and higher harmonics. However, the dynamic performance deteriorates, which affects the final compensation effect.

Aiming at verifying the effectiveness of the proposed SOGI-PLL technology, the study compared and analyzed its performance with SRF-PLL under actual working conditions. The results of simulating the unbalanced voltage condition of the PG using a TP programmable voltage module are showcased in Fig. 7. Figure 7 shows that the B-phase voltage has a standard amplitude of 300 V. Prior to 0.05s, the amplitude of phases A and C decreased by 20% to 240 V. At 0.05s, it further decreased to 210 V, resulting in an increase in imbalance. The TP programmable voltage module can effectively simulate unbalanced working conditions of the PG voltage.



Fig. 7 Results of simulated PG voltage imbalance working condition



Fig. 8 Experimental results under voltage imbalance conditions

The comparison results of the output frequency between traditional SRF-PLL and SOGI based PLL, as well as the output phase waveform of SOGI-PLL, are showcased in Fig. 8. Figure 8 (a) showcases that under the condition of TP imbalance, the output frequency of SRF-PLL exhibits significant fluctuations compared to the standard power frequency, with a fluctuation amplitude of  $\pm 1$  Hz. Its fluctuation range is 49.3-50.7 Hz.



Fig. 9 Detection results of load current and each harmonic current

 Table 3
 Simulation parameters of the system

	,		
Detection method	Computing time/s	Response time/s	Dynamic stability time/s
Continuous fourier transform	3.25	0.47	1.29
Multi-resolution analysis	3.08	0.42	1.37
Adaptive harmonic current detection	2.91	0.51	1.22
This research	2.68	0.34	1.19

According to Fig. 8 (b), the output frequency curve of the PLL on the grounds of SOGI possesses a high smoothness, and it can operate stably within two power frequency cycles, ensuring the accuracy of the output phase. Among them, its output frequency is 47 Hz. Figure 8 (c) shows that the SOGI PLL can complete phase locking within 0.024 s and provide accurate phase information, effectively avoiding the impact of grid voltage imbalance.

According to the harmonic characteristics of the load, it can be seen that when the uncontrolled rectifier bridge is equipped with a resistive load, the harmonics in the PG are mainly concentrated at  $6k \pm 1$  times, and their content shows a decreasing trend with the increase of harmonic frequency. Therefore, this study prioritizes compensating for low order harmonics with high content and significant impact on the PG. Figure 9 displays the detection results of load current and each harmonic current according to the specific HCD model on the grounds of SHRCS established by the research institute. The waveform of the load side current is shown in Fig. 9(a), with a peak current of 10 A. The fluctuation period is 0.02s. Figure 9 (b), 9 (c), and 9 (d) show that, unlike the fundamental detection method, which subtracts the load current from the fundamental component to obtain all HCs, specific HCD on the grounds of SHRCS can directly obtain each HC. Among them, the peak current of the 5th HC is 2 A, and the peak current of the 7th HC is 1 A. In the 11th HC, it not only includes the 11th HC, but also other HCs. According to the principle of HCD, this is mainly related to the cutoff frequency selection of

LPFs. When the cutoff frequency is low, the filtering effect is better, but it also brings significant delay.

To verify the performance of the proposed harmonic detection method, a comparison is conducted with other advanced technologies, including continuous Fourier transform, harmonic detection based on wavelet multi-resolution analysis, and adaptive HCD based on neural networks. The results are presented in Table 3. The proposed method has a calculation time of 2.68s and a response time of 0.34s. It also has a required stability time of only 1.19s under dynamic conditions, indicating its superior performance.

### Analysis of simulation results for parallel APF compensation

Under the application of full harmonic detection method, this study uses the obtained HC as the instruction current. It starts the parallel APF compensation device at 0.05 s, and the waveform of the A-phase grid side current, output compensation current, and command current before and after compensation, as well as the fast Fourier transform (FFT) analysis of the grid side current after compensation, are showcased in Fig. 10. Figure 10 (a) showcases that there is a significant difference in the waveform of the A-phase grid side current before and after compensation. After compensation, the AC side current significantly improves and exhibits a sinusoidal shape. As shown in Fig. 10 (b), after 0.05 s, the actual output compensation current closely follows the command current, indicating the good tracking ability of the output compensation current to the command current. Figure 10(c) shows that the total harmonic distortion (THD) value is 26.58% due to the presence of a harmonic source before compensation. However, after compensation, the THD value significantly decreased to 3.06%, meeting the expected compensation effect. The simulation demonstrates that the active filter structure can accurately detect and filter out harmonic currents in the load, resulting in a sinusoidal grid side current.



Fig. 10 Simulation experiment results of full harmonic compensation

The study continued to explore compensation methods for specific harmonics, with a simulation duration of 0.1 s and a sudden load change occurring at 0.05 s. When using the sum of 5th, 7th, and 11th HCs as the command current for compensation, the compensated A-phase grid side current and FFT analysis are showcased in Fig. 11. As shown in Fig. 11(a), when the load undergoes a sudden change, the distortion of the current waveform increases, while the current amplitude rises from 10 to 18 A. As shown in Fig. 11 (b), the compensated 5th, 7th, and 11th harmonic content is significantly reduced, and the THD rate decreases to 4.08%. This indicates that the algorithm proposed by the research institute can combine various harmonics and use them as instruction currents to filter out specified harmonics or certain harmonics, and selecting the main frequency harmonics for compensation can also meet the system's requirements for harmonic content.

## Conclusion

Currently, as the boost of modern industrial technology, there is a large amount of harmonic pollution in the PG. In response to such problems, a parallel APF is studied and corresponding PLL design and harmonic detection methods are proposed. The study demonstrated that under the condition of TP unbalance, the output frequency of the SRF-PLL fluctuated significantly with respect to the standard power frequency, with a fluctuation amplitude of  $\pm 1$  Hz. The output frequency curve of the PLL based on SOGI exhibited high smoothness, and it can operate stably within two power frequency cycles. These findings suggested that the proposed method has good stability. Meanwhile, SOGI PLL can achieve phase locking within 0.024 s and provide precise phase information. This indicated that the method has better timeliness and accuracy. In cases of TP voltage distortion, the output frequency of the SOGI PLL fluctuated slightly, with a range of only $\pm 0.05$  Hz. The specific HCD method used in SHRCS can directly obtain each HC, unlike the fundamental detection method which subtracts the load current from the fundamental component to obtain all HCs. This indicated that the HCD method is relatively simple to operate and can effectively identify HCs. The fifth HC had a peak current of 2 A, while the seventh HC had a peak current of 1 A. The 11th HC included not only itself but also other HCs. Additionally, the proposed method had a calculation time of 2.68s, a response time of 0.34s, and a required stability time of only 1.19s under dynamic conditions. This indicated that the method is highly computationally efficient and stable. The research institute's parallel APF PLL design and harmonic detection algorithm have shown significant application effects. In practical applications, this method can effectively reduce the impact of harmonics on the PG and improve the quality of electrical



Fig. 11 Simulation experiment results of specific harmonic compensation

energy. However, research primarily focuses on selectively compensating for low-order harmonics with high power content in the system. Further analysis is needed to determine the optimal filtering frequency for achieving the best compensation effect when high-order harmonics are present. Additionally, increasing the inductance value can lead to a deterioration in the system's dynamic performance, resulting in drawbacks in both volume and cost. LCL structures can be used to reduce the impact of switching ripple currents in the future. Currently, APFs are primarily used in low voltage and low current environments. This study explores the combination of APF parallel technology and multi-level technology with specific subharmonic compensation methods for application in medium to high voltage and large capacity environments.

#### Author contributions

Dan Wang wrote the main manuscript text; Linsen Yang validate the research; Lei Ni supervise the research. All authors reviewed the manuscript.

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